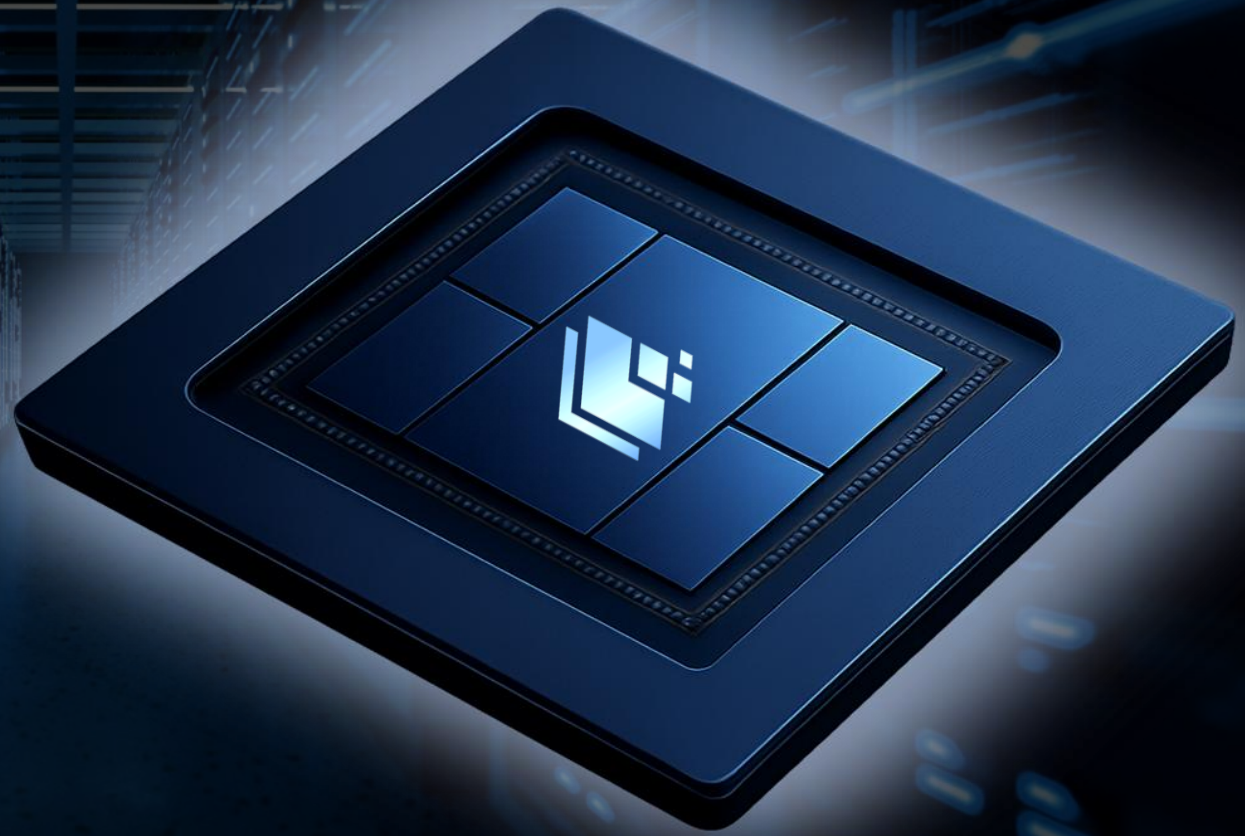
GAONCHIPS

"Designed for Performance. Built on Trust"

GAONCHIPS

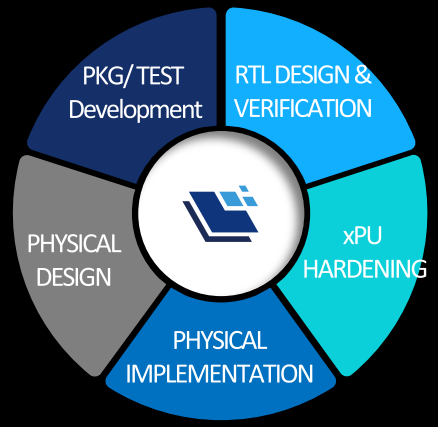


About GAONCHIPS

Samsung Foundry Tier-1 Design Solution Partner

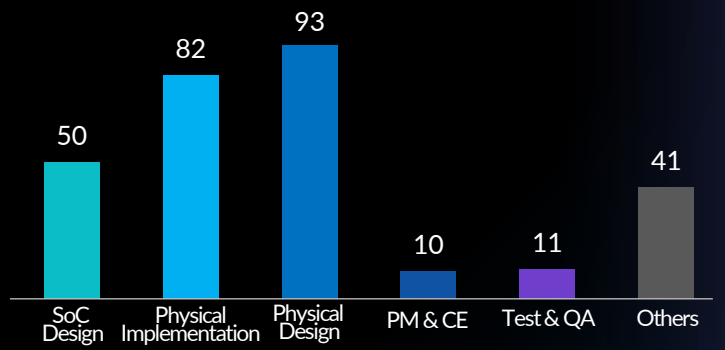
SAMSUNG Foundry Project Tape-outs	SAMSUNG Foundry Technology Experience	SAMSUNG Foundry Partnership	Mass Production Wafer Shipped	Revenue from AI/HPC & Automotive	Revenue from ≤5nm Advanced Nodes
Over 241 Cum.	Up to 2nm SF2/SF2P	Over 12yrs	Over 17,400 28 Project	Over 80%	Over 50%

End-to-End Execution



Engineering Depth

287+ Employees | 85%+ Engineers



Proven Across Key Markets

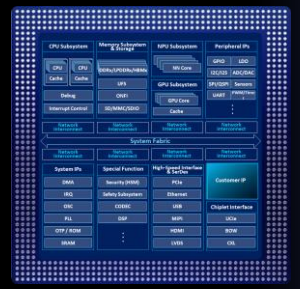
"Designed for Performance. Built on Trust"

Service Coverage

From Design Service to Total Silicon Solution Provider

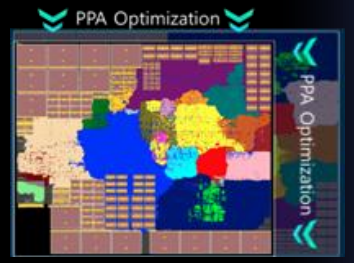
One Partner from Architecture to Mass Production

RTL DESIGN & VERIFICATION



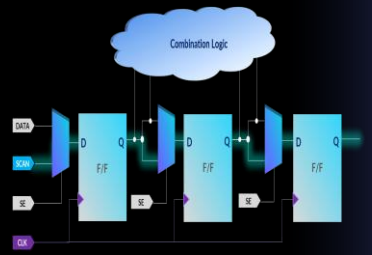
- System Architect
- IP Integration & DV
- FPGA/Emulator Prototyping
- Firmware, Device Driver, BSP
- ISO26262 -compliant Design
- Safety Mechanism

xPU HARDENING



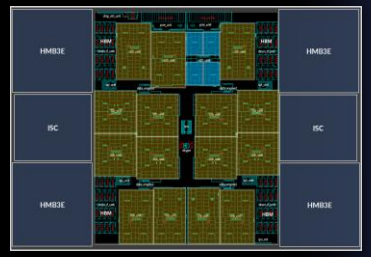
- Systematic Hardening Flow
- Physical-Aware Synthesis
- Broad Arm Processor Experiences

PHYSICAL IMPLEMENTATION



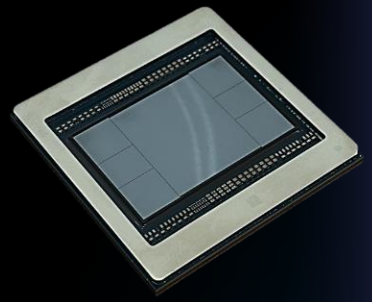
- DFT (SCAN/BIST/JTAG)
- Low Power Design (Clock/Power Gating, SAIF, DVFS, etc.)
- High coverage DFT
- In-system Test

PHYSICAL DESIGN



- Full-Chip Floor Plan
- Physical Layout
- Advanced CTS (for Big-Dies)
- On-chip EM/IR Analysis
- Interposer Design

PKG & TEST



- Package Design Guidelines
- Off-chip PI/SI Analysis
- Test Vector generation
- ATE set-up
- Qualification & Reliability
- AEC-Q100

MASS PRODUCTION

- Full-Turnkey Business (Wafer + PKG + TEST)
- SCM
- eFA/pFA
- IATF16949, PPAP

*Automotive-grade Solutions

Integrated Engineering & Execution by GAONCHIPS

Connected Partnership Ecosystem

One Partner · One Interface · One Connected Ecosystem

Integrated ecosystem enabling full-service ASIC execution through GAONCHIPS

Customer → *Single Interface* → GAONCHIPS

- Faster Time to Market
- Lower Execution Risk
- Turn-key Silicon Delivery

Design Ecosystem

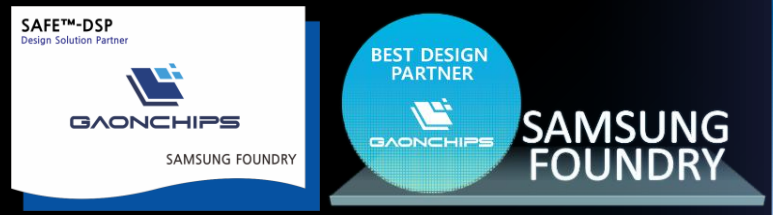
EDA · IP · Verification

arm, Synopsys, Cadence, Siemens, Ansys, Keysight, M31, Rambus, OpenEdges Technology, Inc., Arteris IP, VeriSilicon, ram-sCHIP, MSQUARE, Innosilicon, InPsytech, Qualitas

Foundry & Advanced Manufacturing

Samsung Foundry

Foundry | Advanced Packaging | Memory



Package, Test & Validation

Bump · Package · Test · Validation

Amkor Technology, ASE, HANA MICRON, JCET, SGS, DOOSAN Tesna, ITEK, XILINX, LITBIG, QRT

Bump | Package | Test | EVB/FPGA | Qual Certification

GAONCHIPS Specialty

Differentiated Engineering Expertise Built Through Proven Execution

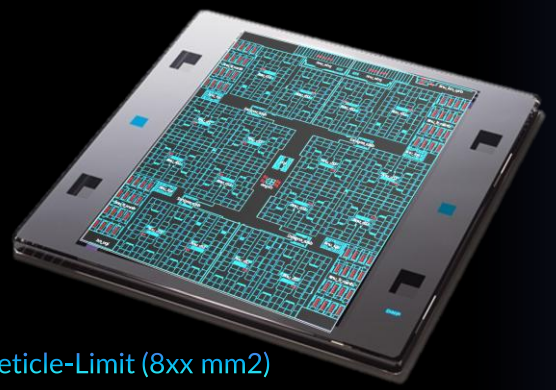
AI/HPC

"The Gateway to Advanced Node & Packaging"

Scale Complexity

Big-Die + Advanced Package Design

- 800mm²+ Reticle-Limit Design
- 1kW-Class Power Delivery
- 2.5D/3D Package · HBM Integration



Reticle-Limit (8xx mm2)

Edge AI

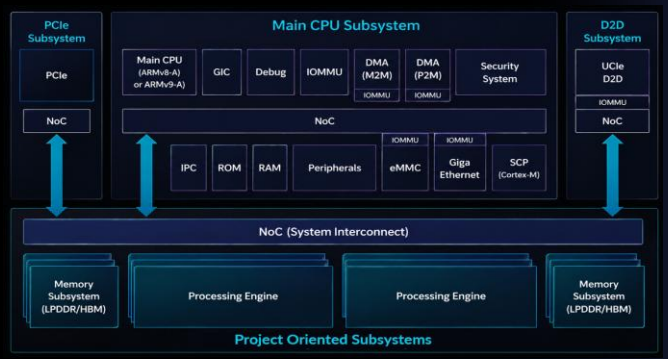
"Accelerating Time-to-Market for On-Device / Physical AI"

Optimize Efficiency

Full-Stack Low Power Design Flow:

- Si-Proven AI Platform: GP1000™
- AI-Driven Physical Design Methodology
- Early Power / Performance Estimation

Low Power AI Platform: GP1000™



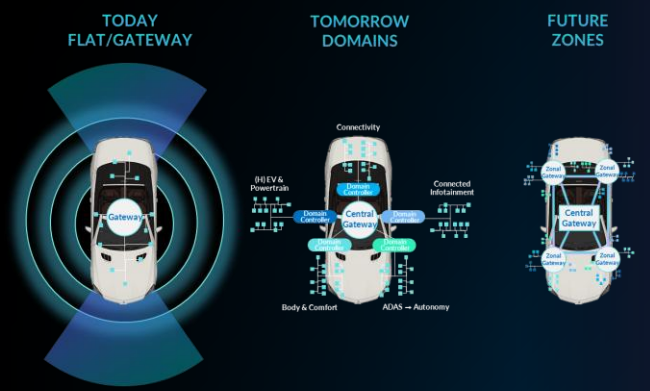
Automotive

"Proven Reliability for the Next-Gen SDV Era"

Assure Reliability

Proven Mass Production Track Record

- Long-term Global OEM Partner (8/5nm)
- Turn-key Design / Advanced DFT
- arm Automotive Project Partner



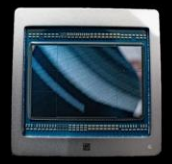
Project Portfolio

High-growth market-oriented project portfolio

Automotive Heritage with various design experiences and competitiveness
(Robust Design, Advanced DFT (Inc. In-system Test), Etc.)
Ramp up the AI-enabled HPC market

2nm

The world's largest AI accelerator @ Samsung 2nm GAA process



Samsung's 2.5D Package Technology I-Cube5™

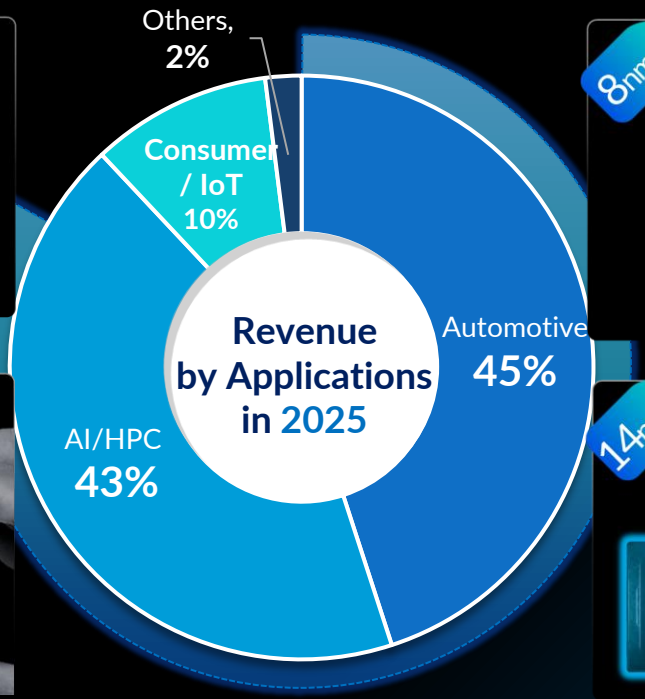
8xx mm² Reticle-limited Die Size
+15 Billion Gate Counts, +3 Billion Instances

2.5D Package with HBM3E x4
32GB x4, 9.2Gbps, Off-chip PI/SI Sign-off

Advanced Physical Implementation
ML* based Physical Implementation, Advanced CTS, Source synchronous clocking, etc.
* Machine learning

5nm

Marks a Magnificent Step in Cutting-Edge Solutions
DX-M1: Ultra Efficient AI Chip Wins CES Innovation Award



8nm

Mid-Low Infotainment/Cockpit Solution
Hypervisor-less, SDR(Software Defined Radio), STR

Dolphin5

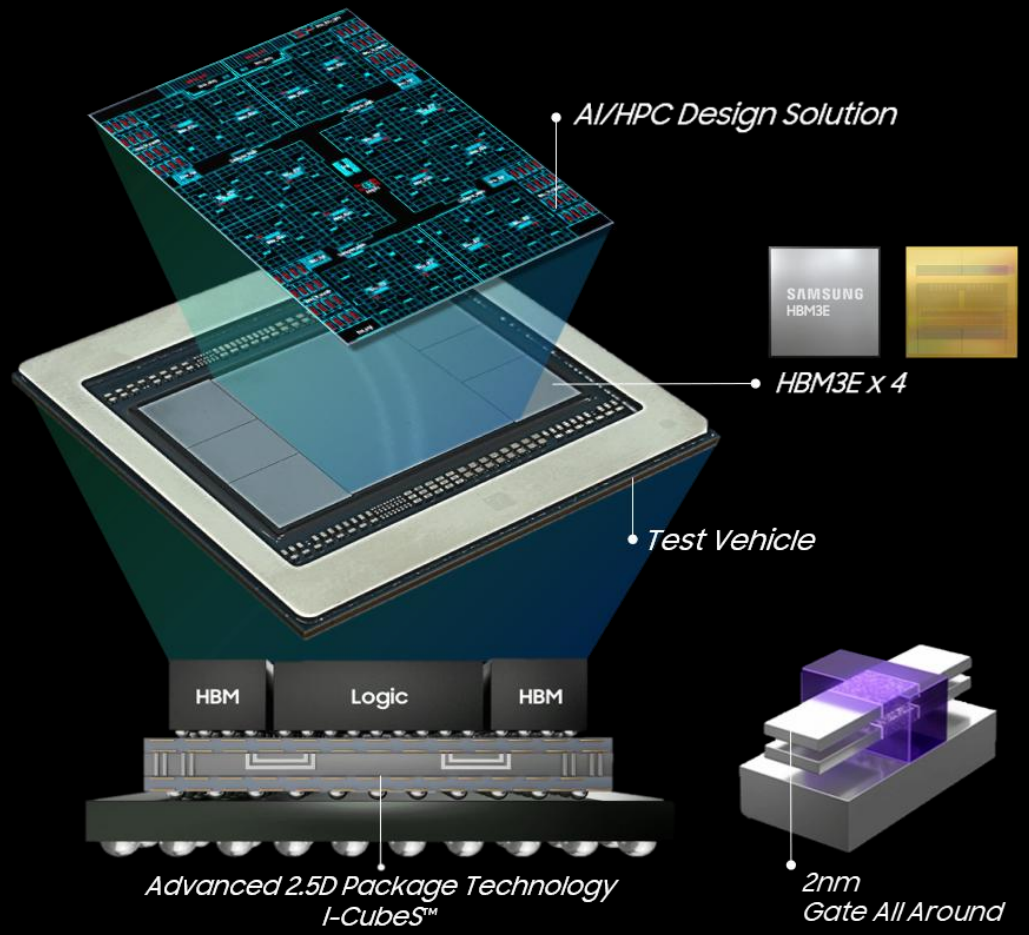
14nm

Driving Innovation in Next-Generation ADAS Processor
APACHE6: Advancing Safe Autonomous Driving

Domain controller for Euro NCAP-ready ADAS L2/L2+ Solution

Proven Execution at the Leading Edge

Real-World Samsung Foundry 2nm GAA · Reticle-Limit AI/HPC · Advanced 2.5D/HBM



8xx mm² Die Area	**15 Billion** Total Gate Count	**3 Billion** Total Instances
Advanced 2.5D Integration Turnkey Solution with integrated Si-interposer	**Forefront of Next Gen. Process** Samsung Foundry 2nm Gate-All- Around	**AI-Driven Optimization** Enhancing Chip Design with LLMs & Generative AI

Key Implementation Feature

Reticle-limited Large-die Implementation

- HW/SW infrastructure for extremely large-scale design
- Distributed computing, Advanced CTS, ML based optimization, etc.

2.5D Off-Chip PI/SI signoff

- interposer-inclusive HBM interface validation up to 9.6Gbps

Source Synchronous clocking

- Low latency / High performance across the NoC

GP1000™ AI/HPC Platform

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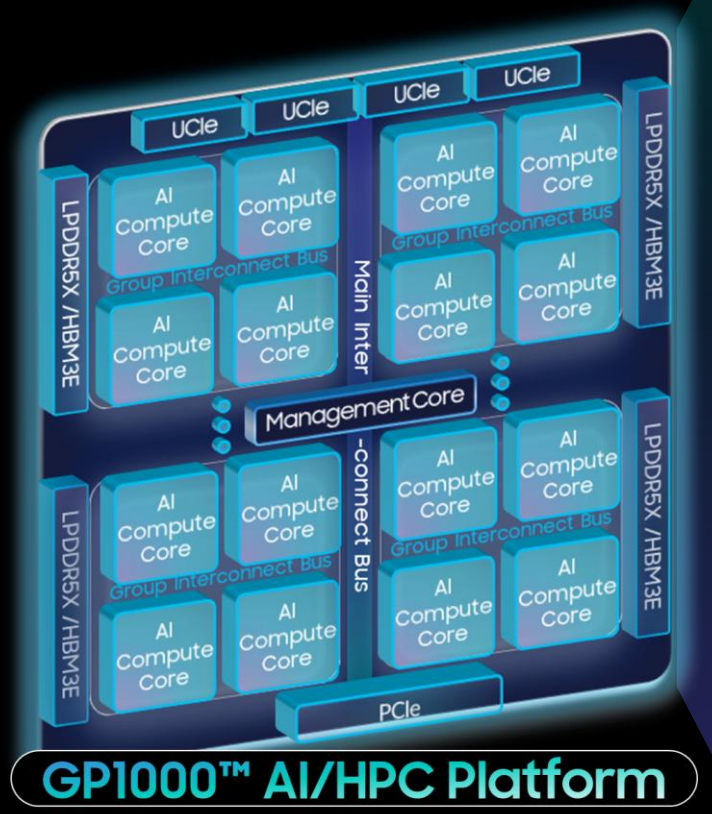


Main Features

Management Core

System BUS

FlexNoC

Die to Die Interface

UCIe™ Universal Chiplet Interconnect Express

Memory

LPDDR5x
(up to 32-bit x 8-ch)

HBM3E (up to 4ea)

Security

Caliptra, IDE for PCIe

Advanced Interface

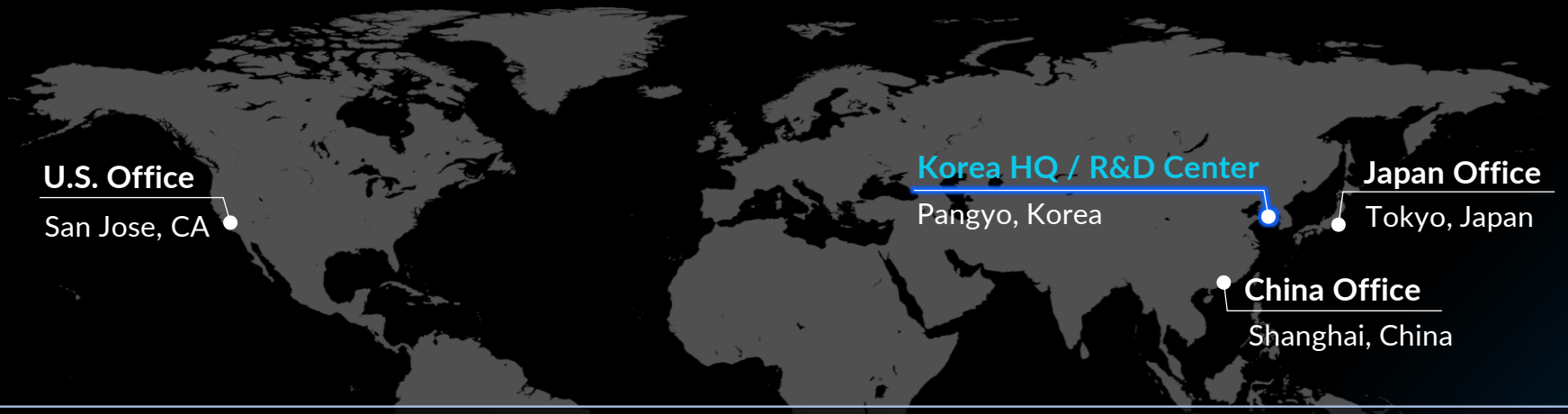
PCIe Gen5

Deliverables & Support

for Evaluation
- Encrypted RTL
- Device Driver
- FPGA Prototyping @Zephyr OS Embedded

for Production (Turnkey)
- 2.5D/3D Advanced PKG & Interposer Design
- PI/SI Analysis
- Memory (HBM)

Global Network

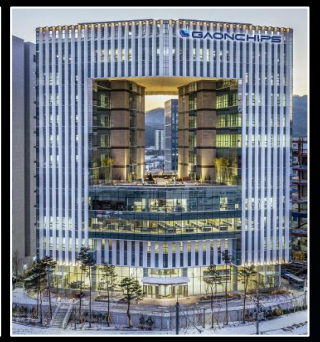


One Team, One GAONCHIPS

Seamless collaboration from engagement to execution

America in San Jose

Korea R&D Center / HQ in Pangyo



Engineering Execution Hub

China in Shanghai

Japan in Tokyo

More information
SCAN
To Save

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GAONCHIPS

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www.GAONCHIPS.com

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